UNITED STATES PATENT APPLICATION

OF

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FOR

LIQUID CRYSTAL DISPLAY DEVICE

[0001] This application claims the benefit of Korean Application No. P2000-86846 filed on December 30, 2000, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a liquid crystal display, and more particularly, to a liquid crystal display device for maintaining a picture quality in a divisional driving mode for a large-scale/high-resolution liquid crystal display panel.

Discussion of the Related Art

[0003] Generally, a liquid crystal display (LCD) controls light transmittance of liquid crystal cells arranged in a matrix pattern in response to video signals, thereby displaying a picture corresponding to the video signals on the liquid crystal display panel.

[0004] To this end, the LCD includes an active area having liquid crystal cells arranged in an active matrix type and driving circuits for driving the liquid crystal cells at the active area. More specifically, the LCD includes upper and lower plates. A plurality of thin film transistors (TFT's) for switching the liquid crystal cells, driving circuits for driving the thin film

transistors and signal lines connected between the driving circuits and the TFT's are mounted on the lower substrate. The upper plate is provided with color filters separated for each cell area by black matrix stripes in correspondence with the matrix liquid crystal cells and transparent electrodes coated on the color filters, and spacers provided between the upper and lower plates to maintain a constant cell gap. A liquid crystal is filled in a space defined between the upper and lower plates by the spacers.

[0005] Such an LCD is fabricated by separately preparing the upper plate and the lower plate. After the two plates are attached to each other, a liquid crystal is injected between the plates through a liquid crystal injection hole. Thereafter, the LCD is completed by coating the liquid crystal injection hole with a sealant and curing the sealant.

[0006] The driving circuits require a plurality of driving integrated circuits (D-IC) connected to a plurality of data lines and gate lines to apply data signals and a scanning signal to the data lines and the gate lines, respectively. As the LCD is capable of realizing a large scale and a high resolution, a display speed of the liquid crystal display panel becomes slow because the time required for allowing the D-IC to conduct all

the TFT's is extended. For this reason, when a gate voltage level is set to be too high, a voltage drop occurs from a pixel due to a feed through phenomenon, upon turning off the gate voltage, thereby causing a more serious distortion in picture quality.

[0007] Accordingly, there is a demand for a divisional driving of the liquid crystal display panel to overcome the problem as discussed above.

[0008] In such a divisional driving method for the liquid crystal display panel, as shown in FIG. 1, each data lines of the panel is physically cut at the half point "A" in FIG. 1.

[0009] In FIG. 1, the conventional LCD includes TFT's provided at the intersections between a plurality of gate lines 7 and 9 and data lines 3 and 5, upper and lower source drive IC's (SD-IC) 2 and 4 for applying data signals to the data lines 3 and 5 physically divided into the upper side and the lower side. Left and right gate drive IC's (GD-IC) 6 and 8 applies scanning signals to the upper and lower gate lines 7 and 9 that are divided only based on a signal without a physical division.

[0010] The upper SD-IC 2 applies the data signals to the data lines 3 of the first divided panel positioned at the upper portion of the panel in which the data lines 3 and 5 are cut at the half point "A" of the panel. The lower SD-IC 4 applies the

data signals to the data lines 5 of the second divided panel positioned at the lower portion of the panel in which the data lines 3 and 5 are cut at the half point "A" of the panel.

[0011] The left GD-IC 6 and the right GD-IC 8 apply scanning signal to the upper and lower gate lines 7 and 9 to turn on the TFT's.

[0012] In the LCD, in order to display a picture on each pixel, data signals are applied from the upper and lower SD-IC 2 and 4 to the data lines 3 and 5. Scanning signals from the left and right GD-IC 6 and 8 are sequentially applied to the gate lines 7 and 9 crossing the data lines 3 and 5 to turn on the TFT's. Accordingly, the data signal is applied through source and drain electrodes of the TFT to the pixel electrode, thereby displaying a picture on each pixel.

[0013] The upper and lower data lines 3 and 5 are driven independently as shown in FIG. 2. Thus, upon implementing the images, a difference in the picture quality is caused between the first divided panel and the second divided panel. More specifically, the TFT's on the panel improve a sustaining characteristic of the data signals applied to the pixels with the aid of storage capacitors (not shown). Also, the TFT's stabilize

a gray scale display and maintain pixel information while the pixels are in a non-selection interval.

[0014]The storage capacitors connected to the pixels of the first divided panel are connected to the pre-stage gate lines to charge applied voltages. On the other hand, the storage capacitors connected to the first pixels of the second divided panel cannot charge voltages from the pre-stage gate lines at the non-selection interval because no pre-stage gate line at the storage capacitors is caused by the vertical division. As a result, there is a difference in a picture quality between the first divided panel and the second divided panel.

[0015]Moreover, the conventional LCD has an additional problem in that a circuitry configuration becomes complicated since a frame memory should be used as a panel driving apparatus for a divisional driving.

SUMMARY OF THE INVENTION

[0016]Accordingly, the present invention is directed to a liquid crystal display device that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

[0017]Another object of the present invention is to provide a liquid crystal display device for maintaining a picture quality

in divisional driving of a large-scale/high-resolution liquid crystal display panel.

[0018]Additional features and advantages of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0019]To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a liquid crystal display device includes a liquid crystal display panel having a plurality of liquid crystal cells at each intersection between a plurality of data lines and gate lines and a plurality of thin film transistors driving the liquid crystal cells, a plurality of switching devices at least one of at the data lines and the gate lines switching to either a divisional driving mode or a non-divisional driving mode, a controller supplying a control signal to the switching devices to control the switching devices, and a control line connecting the switching devices and the controller.

[0020] In the liquid crystal display device, the switching devices include a plurality of first switching devices at the middle portion of the data lines, and a plurality of second switching devices at the middle portion of the gate lines.

[0021] In the liquid crystal display device, the control signal is either an on-selection signal for the divisional driving mode or an off-selection signal for the non-divisional driving mode.

[0022] In another aspect of the present invention, a liquid crystal display device includes a liquid crystal display panel having a plurality of liquid crystal cells at each intersection between a plurality of data lines and gate lines and a plurality of thin film transistors driving the liquid crystal cells, a plurality of switching devices at least one of at the data lines and the gate lines switching to either a divisional driving mode or a non-divisional driving mode, a controller supplying a control signal to the switching devices to control the switching devices, a control line connecting the switching devices and the controller, first and second source drivers applying a data signal to the data lines, first and second gate drivers applying a gate signal to the gate lines, and a timing controller applying a control signal to the source driver and the gate driver.

[0023] In the liquid crystal display device, the switching devices include a plurality of first switching devices at the middle portion of the data lines, and a plurality of second switching devices at the middle portion of the gate lines.

[0024] In the liquid crystal display device, the control signal is either an on-selection signal of the divisional driving mode or an off-selection signal of the non-divisional driving mode.

[0025] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the invention and together with the description serve to explain the principle of the invention.

[0027] In the drawings:

[0028] FIG. 1 is a schematic plan view for showing a divisional driving scheme in a conventional liquid crystal display panel;

[0029] FIG. 2 is an enlarged plan view of the "A" portion in FIG. 1;

[0030] FIG. 3 is a block diagram showing a two-divisional driving scheme in a liquid crystal display according to a first embodiment of the present invention;

[0031] FIG. 4 is a plan view of the divisional driving switching device provided at the center of the data line in FIG. 3;

[0032] FIG. 5 is a block diagram showing a four-divisional driving scheme in a liquid crystal display according to a second embodiment of the present invention; and

[0033] FIG. 6 is a plan view of the divisional driving switching device provided at the center of the data line in FIG. 5.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0034] Reference will now be made in detail to the illustrated embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0035] FIG. 3 illustrates a liquid crystal display (LCD) according to a first embodiment of the present invention.

[0036] The LCD in FIG. 3 includes a liquid crystal display panel 67 having a plurality of gate lines 37 and 39 and data lines 33 and 35 divided into the upper and lower sides that cross each other. TFT's are provided at the intersections therebetween to

drive liquid crystal cells Clc. Upper and lower source drivers 32 and 34 apply data signals to the upper and lower data lines 33 and 35 of the liquid crystal display panel 67. Left and right gate drivers 36 and 38 apply scanning signals to the gate lines 37 and 39. A divisional driving switching device "B" provided at the divided point between the upper and lower data lines 33 and 35 to select a divisional driving mode and a non-divisional driving mode. A timing controller 61 is supplied with digital video data and horizontal and vertical synchronizing signals H and V. A divisional driving controller 53 applies a selection signal for one of the divisional driving mode and the non-divisional driving mode to the divisional driving switching device "B".

[0037] In the liquid crystal display panel 67, a liquid crystal is injected between two glass substrates, and the upper and lower gate lines 37 and 39 are provided on the lower glass substrate in such a manner to perpendicularly cross the data lines 33 and 35 divided into the upper side and the lower side.

[0038] The TFT's provided at the intersections between the data lines 33 and 35 and the gate lines 37 and 39 apply the data signals through the data lines 33 and 35 to the liquid crystal cells Clc in response to the scanning pulses. To this end, gate

electrodes of the TFT's are connected to the gate lines 37 and 39 while source electrodes thereof are connected to the data lines 33 and 35. Drain electrodes of the TFT's are connected to the pixel electrodes of the liquid crystal cells Clc.

[0039]The timing controller 61 rearranges digital video data supplied from a digital video card (not shown). Red(R), green(G), and blue(B) data RGB rearranged by the timing controller 61 are applied to the upper and lower source drivers 32 and 34. Further, the timing controller 61 generates timing control signals, such as a dot clock DCLK, a gate start pulse GSP, a gate shift clock GSC and an output enable/disable signal, and a polarity control signal in accordance with the horizontal and vertical synchronizing signals H and V inputted thereto, thereby controlling the upper and lower source drivers 32 and 34 and the left and right gate drivers 36 and 38. The dot clock DCLK and the polarity control signal are applied to each of the upper and lower source drivers 32 and 34 while the gate start pulse GSP and the gate shift clock GSC are applied to each of the left and right gate drivers 36 and 38.

[0040]Each of the left and right gate drivers 36 and 38 includes a shift register for sequentially generating a scanning pulse, that is, a gate high pulse in response to the gate start pulse

GSP and the gate shift clock GSC from the timing controller 61, and a level shifter for shifting a voltage of the scanning pulse into a level suitable for driving the liquid crystal cell Clc. The TFT is turned on in response to the scanning pulse. Upon turning on the TFT, data signals on the upper and lower data lines 33 and 35 are applied to the pixel electrode of the liquid crystal cell Clc.

[0041]Each of the left and right gate drivers 36 and 38 is mounted with a plurality of gate drive IC's (GD-IC) for applying scanning signals to the gate lines 37 and 39 each having a block unit. Each of the GD-IC sequentially applies the scanning signal to the gate lines 37 and 39 connected thereto.

[0042]The left and right gate drivers 36 and 37 apply a bilateral scanning signal to the gate lines 37 and 39 of the first and second divided panels that are divided into the upper side and the lower side based on a signal only without a physical division. They are arranged at the left side and the right side of the liquid crystal display panel 67 so as to reduce a line resistance of the gate lines 37 and 39, and apply the scanning signals to the gate lines 37 and 39.

[0043]The upper and lower source drivers 32 and 34 are supplied with the red(R), green(G), and blue(B) data RGB, and receive the

dot clock DCLK from the timing controller 61. The upper and lower source drivers 32 and 34 sample the R, G, and B data RGB in response to the dot clock DCLK, and then latch the sampled data line by line. The latched data are converted into analog data and simultaneously applied to the upper and lower data lines 33 and 35 at each scanning interval. The upper and lower source drivers 32 and 34 may supply gamma voltages according to data signals to the upper and lower data lines 33 and 35.

[0044] Each of the upper and lower source drivers 32 and 34 is mounted with a plurality of source drive IC's (SD-IC) for applying data signals to the data lines 33 and 35 each having a block unit. Each of the SD-IC sequentially applies a data signal to the data lines 33 and 35 connected thereto. In other words, the data signals from the upper source driver 32 are applied to the data lines 33 of the first divided panel positioned at the upper side of the liquid crystal display panel 67, whereas the data signals from the lower source driver 34 are applied to the data lines 35 of the second divided panel positioned at the lower side of the liquid crystal display panel 67.

[0045] The divisional driving switching device "B" is arranged between the upper and lower data lines 33 and 35 divided, as shown in FIG. 4. The divisional driving switching device "B"

switches a divisional driving mode and a non-divisional driving mode of the liquid crystal display panel 67 divided by the upper side and the lower side in accordance with a selection signal applied from the divisional driving controller 63. To this end, a gate electrode of the divisional driving switching device "B" is connected to a divisional driving control line 41 while a source electrode thereof is connected to the upper data line 33. A drain electrode of the divisional driving switching device "B" is connected to the lower data line 35.

[0046]Accordingly, the divisional driving switching device "B" allows the data signals supplied from the upper source driver 32 to the upper data lines 33 to be applied to the lower data lines 35 in response to a selection signal for a non-divisional driving mode of the liquid crystal display panel 67 from the divisional driving controller 63. Further, the upper data lines 33 and the lower data lines 35 are disconnected by the divisional driving switching device "B" in response to the selection signal for the divisional driving mode of the liquid crystal display panel 67 from the divisional driving controller 63. Thus, the upper data lines 33 receive data signals from the upper source driver 32 while the lower data lines 35 receive data signals from the lower source driver 34.

[0047] The divisional driving controller 63 applies an ON/OFF selection signal to the divisional driving switching device "B" by an externally selected ON/OFF signal. In other words, the liquid crystal display panel 67 is driven in a non-divisional driving mode for an on-selection signal, whereas it is driven in a divisional driving mode for an off-selection signal.

[0048] In the present LCD, the divisional driving switching device "B" is arranged at the center of the data line of the liquid crystal display panel and is subject to an external ON/OFF control, so that the liquid crystal display panel 67 can be driven in both the divisional driving mode and the non-divisional driving mode.

[0049] FIG. 5 illustrates a liquid crystal display (LCD) according to a second embodiment of the present invention.

[0050] The LCD in FIG. 5 includes a liquid crystal display panel 77 having four-divided gate lines 51, 53, 55, and 57 and four-divided data lines 43, 45, 47, and 49 that cross each other and TFT's provided at the intersections therebetween to drive liquid crystal cells Clc. Upper and lower source drivers 42 and 44 apply data signals to the upper data lines 43 and 45 and the lower data lines 47 and 49 of the liquid crystal display panel 77. Left and right gate drivers 46 and 48 apply scanning signals to

the left gate lines 51 and 55 and the right gate lines 53 and 57. A first divisional driving switching device "C" provided at the middle portion of the upper data lines 43 and 45 and the lower data lines 47 and 49 selects a vertical divisional driving mode or a non-divisional driving mode. A second divisional driving switching device "D" provided at the middle portion of the left gate lines 51 and 55 and the right gate lines 53 and 57 selects a horizontal divisional driving mode or a non-divisional driving mode. A timing controller 81 is supplied with a digital video data and horizontal and vertical synchronizing signals H and V. A divisional driving controller 83 applies a selection signal for one of the vertical/horizontal divisional driving mode and the non-divisional driving mode to the first and second divisional driving switching devices "C" and "D".

[0051] In the liquid crystal display panel 77, a liquid crystal is injected between two glass substrates, and the gate lines 51, 53, 55, and 57 are provided on the lower glass substrate in such a manner to perpendicularly cross the data lines 43, 45, 47, and 49.

[0052] The TFT's provided at the intersections between the data lines 43, 45, 47, and 49 and the gate lines 51, 53, 55, and 57 apply data signals through the data lines 43, 45, 47, and 49 to the liquid crystal cells Clc in response to the scanning pulses.

To this end, gate electrodes of the TFT's are connected to the gate lines 51, 53, 55, and 57 while source electrodes thereof are connected to the data lines 43, 45, 47, and 49. Drain electrodes of the TFT's are connected to the pixel electrodes of the liquid crystal cells Clc.

[0053] The timing controller 81 rearranges digital video data supplied from a digital video card (not shown). Red(R), green(G), and blue(B) data RGB rearranged by the timing controller 81 are applied to the upper and lower source drivers 42 and 44. Further, the timing controller 81 generates timing control signals, such as a dot clock DCLK, a gate start pulse GSP, a gate shift clock GSC and an output enable/disable signal, and a polarity control signal in accordance with the horizontal and vertical synchronizing signals H and V inputted thereto, thereby controlling the upper and lower source drivers 42 and 44 and the left and right gate drivers 46 and 48. The dot clock DCLK and the polarity control signal are applied to each of the upper and lower source drivers 42 and 44 while the gate start pulse GSP and the gate shift clock GSC are applied to each of the left and right gate drivers 46 and 48.

[0054] Each of the left and right gate drivers 46 and 48 includes a shift register for sequentially generating a scanning pulse,

that is, a gate high pulse in response to the gate start pulse GSP and the gate shift clock GSC from the timing controller 81, and a level shifter for shifting a voltage of the scanning pulse into a level suitable for driving the liquid crystal cell Clc. The TFT is turned on in response to the scanning pulse. Upon turning on the TFT, the data signals on the upper and lower data lines 43 and 45 are applied to the pixel electrode of the liquid crystal cell Clc.

[0055] Each of the left and right gate drivers 46 and 48 is mounted with a plurality of gate drive IC's (GD-IC) for applying scanning signals to the gate lines 51, 53, 55, and 57 each having a block unit. Each of the GD-IC sequentially applies the scanning signal to the gate lines 51, 53, 55, and 57 connected thereto.

[0056] The upper and lower source drivers 42 and 44 are supplied with the red(R), green(G), and blue(B) data RGB, and receive the dot clock DCLK from the timing controller 81. The upper and lower source drivers 42 and 44 sample the R, G, and B data RGB in response to the dot clock DCLK, and then latch the sampled data line by line. The latched data is converted into analog data and simultaneously applied to the upper data lines 43 and 45 and the lower data lines 47 and 49 at each scanning interval. The upper

and lower source drivers 42 and 44 may apply gamma voltages according to data signals to the upper data lines 43 and 45 and the lower data lines 47 and 49.

[0057] Each of the upper and lower source drivers 42 and 44 is mounted with a plurality of source drive IC's (SD-IC) for applying data signals to the data lines 43, 45, 47, and 49 each having a block unit. Each of the SD-IC sequentially applies a data signal to the data lines 43, 45, 47, and 49 connected thereto.

[0058] In accordance with the left and right gate driver 46 and 48 and the upper and lower source drivers 42 and 44, the first divided panel positioned at the left upper side of the liquid crystal display panel 77 is driven by the upper source driver 42 and the left gate driver 46. The second divided panel positioned at the right upper side of the liquid crystal display panel 77 is driven by the upper source driver 42 and the right gate driver 48. The third divided panel positioned at the left lower side is driven by the lower source driver 44 and the left gate driver 46. The fourth divided panel positioned at the right upper side is driven by the lower source driver 42 and the right gate driver 48.

[0059] The first divisional driving switching device "C" is arranged between the upper data lines 43 and 45 and the lower

data lines 47 and 49, as shown in FIG. 4, whereas the second divisional driving switching device "D" is provided at the middle portion of the left gate lines 51 and 55 and the right gate lines 53 and 57, as shown in FIG. 6.

[0060]The first divisional driving switching device "C" switches a vertical divisional driving mode to a vertical non-divisional driving mode, and vice versa, of the liquid crystal display panel 77 divided into the upper side and the lower side in accordance with a selection signal applied from the divisional driving controller 83. To this end, a gate electrode of the first divisional driving switching device "C" is connected to a vertical divisional driving control line 50 while a source electrode thereof is connected to the upper data lines 43 and 45. A drain electrode of the first divisional driving switching device "C" is connected to the lower data lines 47 and 49.

[0061]Accordingly, the first divisional driving switching device "C" allows the data signals supplied from the upper source driver 42 to the upper data lines 43 and 45 to be applied to the lower data lines 47 and 49 in response to a selection signal for a vertical non-divisional driving mode of the liquid crystal display panel 77 from the divisional driving controller 83. Further, the first divisional driving switching device "C"

electrically separates the upper data lines 43 and 45 from the lower data lines 47 and 49 in response to a selection signal for a vertical divisional driving mode of the liquid crystal display panel 77 from the divisional driving controller 83. Thus, the upper data lines 43 and 45 receive data signals from the upper source driver 42 while the lower data lines 47 and 49 receive data signals from the lower source driver 44.

[0062]Referring to FIG. 6, the second divisional driving switching device "D" switches a horizontal divisional driving mode to a horizontal non-divisional driving mode, and vice versa, of the liquid crystal display panel 77 divided into the left side and the right side in accordance with a selection signal applied from the divisional driving controller 83. To this end, a gate electrode of the second divisional driving switching device "D" is connected to a horizontal divisional driving control line 52 while a source electrode thereof is connected to the left gate lines 51 and 55. A drain electrode of the second divisional driving switching device "D" is connected to the right gate lines 53 and 57.

[0063]Accordingly, the second divisional driving switching device "D" allows the data signals supplied from the left gate driver 46 to the left gate lines 51 and 55 to be applied to the right gate

lines 53 and 57 in response to a selection signal for a horizontal non-divisional driving mode of the liquid crystal display panel 77 from the divisional driving controller 83. Further, the second divisional driving switching device "D" electrically separates the left gate lines 51 and 55 from the right gate lines 53 and 57 in response to a selection signal for a horizontal divisional driving mode of the liquid crystal display panel 77 from the divisional driving controller 83. Thus, the left gate lines 51 and 53 receive data signals from the left gate driver 46 while the right gate lines 53 and 57 receive data signals from the right gate driver 48.

[0064] The divisional driving controller 83 applies an ON/OFF selection signal to each of the first and second divisional driving switching devices "C" and "D" by an externally selected ON/OFF signal. In other words, the liquid crystal display panel 77 is driven in a non-divisional driving mode when all the selection signals applied to the first and second divisional driving switching devices "C" and "D" are an on-selection signal. On the other hand, the liquid crystal display panel 77 is driven in a divisional driving mode when all the selection signals applied to the liquid crystal display panel 77 are an off-selection signal. As a result, the liquid crystal display panel

77 is driven based on four-divisions in the vertical and horizontal directions.

[0065] In the mean time, when a selection signal applied to the first divisional driving switching device "C" is an ON signal and a selection signal applied to the second divisional driving switching device "D" is an OFF signal, the liquid crystal display panel 77 is driven based on two-divisions in the horizontal direction. On the other hand, when a selection signal applied to the first divisional driving switching device "C" is an OFF signal and a selection signal applied to the second divisional driving switching device "D" is an ON signal, the liquid crystal display panel 77 is driven based on two-divisions in the vertical direction.

[0066] In the present LCD, the liquid crystal display panel 77 is divided into four areas in the vertical and horizontal directions. The first and second divisional driving switching devices "C" and "D" provided at the middle portion of the divided data lines and the divided gate line are controlled. Thus, a four-divisional driving mode, a two-divisional driving mode, and a non-divisional driving mode are realized in the present invention. Accordingly, the same driving voltage is applied to the same line, so that a deterioration in picture quality between the upper and lower

sides and the left and right sides of the liquid crystal display panel is prevented.

[0067]As described above, the thin film transistors in the present invention are further provided at the physically divided data lines, so that either a divisional driving mode or a non-divisional driving mode is selected based on a signal. Furthermore, the same driving voltage is applied to the signal lines by the divisional driving system, thereby solving a problem in picture quality caused by a signal line resistance in a large-scale/high-resolution LCD panel.

[0068]It will be apparent to those skilled in the art that various modifications and variations can be made in the liquid crystal display device of the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.